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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,189	09/24/2003	Vipul Srivastava	16869Q-088700US	6394

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EXAMINER	
ALPHONSE, FRITZ	

ART UNIT	PAPER NUMBER
2112	

MAIL DATE	DELIVERY MODE
10/15/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/671,189	SRIVASTAVA, VIPUL	
	Examiner	Art Unit	
	Fritz Alphonse	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 13-19* is/are rejected.

7)☒ Claim(s) *12,20 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

0.1 This Office Action is in response to the amendment filed on 8/03/2007. Claims 1-21 are pending.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-11, 13-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murai (U.S. Pat. No. 4,866,717) and Frederickson (U.S. Pat. No. 5,805,799) in view of Tamai (U.S. Pat. No. 6,799,283) and further in view of Hashemi (U.S. Pat. No. 6,981,171).

As to claim 1, Murai (figs. 1-2) shows a data storage system including a controller that generates a sector of data from an old logical block address to a new logical block address when a portion of a data storage medium corresponding to the old LBA contains a defect (col. 3, lines 36-58) and a cycle redundancy check engine that generates old cyclic redundancy check bytes based on the old LBA (col. 6, lines 35-54).

Murai does not explicitly disclose a controller that reassigns a sector of data from an old logical block address (LBA) to a new logical block address. However, the limitation is obvious and well known in the art, as evidenced by Tamai (figs. 13, 14; col. 17, lines 7-18).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine Murai's code error detecting apparatus with the disk array device, as disclosed by Tamai. Doing so would provide a disk array device capable of reading data from a

disk array to transmit the same to a host device and writing data from the host device in the disk array in a short period of time.

Murai does not explicitly disclose a CRC that performs an exclusive OR (XOR) function on the LBA and a Galois Field multiplication on a result of the first XOR function, and performs a second XOR function on a result of the Galois Field multiplication.

However, in the same field of endeavor, Frederickson (fig. 4) discloses data integrity code including logical block address including a CRC that performs Galois Field multiplication on a result of the first XOR function, and performs XOR function on a result of the Galois Field multiplication (col. 2, lines 37-47; col. 10, lines 60 through col. 11 line 38).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine Murai's code error detecting apparatus with the data integrity device, as disclosed by Frederickson. Doing so would reduce the miscorrection probability of an error correction process carried out in accordance with an ECC (col. 2, lines 10-13).

In addition, as to claim 1, Murai and Frederickson does not explicitly disclose an old cyclic redundancy check bytes to generate updated cyclic redundancy check bytes that are based on the new LBA.

However, the limitation is obvious and well known in the art, as evidenced by Hashemi (col. 7, lines 45 through col. 8 line 2; col. 8, lines 47-62).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to improve upon the data storage device, as disclosed by Hashemi. Doing so would improve fault tolerance that may be achieved by checking LBA/CRC information within host interface and either the memory controller or disk interface.

As to claims 2-4, Murai (fig. 1) discloses a data storage system comprising a memory buffer (fig. 1A, 107), wherein the CRC engine (101) writes the updated cyclic redundancy check bytes to the memory buffer (106), and wherein the sector of data and the LBA contain bytes (col. 6, lines 25-54).

As to claim 5-7, 13-14, Murai (fig. 1) discloses a data storage system, a controller is configured to store data onto a magnetic hard disk (col. 8, lines 39-53).

As to claim 8, method claim 8 corresponds to apparatus claim 1; therefore, it is analyzed as previously discussed in claim 1 above.

As to claims 9-11, method claims 9-11 correspond to apparatus claims 2 and 4; therefore, they are analyzed as previously discussed in claims 2 and 4 above.

As to claim 15, Murai (fig. 1) discloses a disk drive error correction system (col. 8, lines 39-53) including a cycle redundancy check engine that generates old cyclic redundancy check bytes based on a first logic block address (LBA) for a sector of data (col. 6, lines 25-54).

Murai does not explicitly disclose XOR gates that performs a first exclusive OR (XOR) function on the old LBA and the new LBA; circuitry for performing Galois Field multiplication on a result of the first XOR function LBA.

However, these limitations are obvious and very well known in the art, as evidenced by Frederickson (fig. 4). See the motivation for the same reason disclosed in claim 1 above.

In addition, as to claim 15, the use of XOR gates performing exclusive OR (XOR) function on LBA circuitry is clearly disclosed by Biskup (U.S. Pat. No. 6,751,757). See figure 7A and column 11, lines 14-32.

As to claims 16-17, Murai (fig. 1) discloses a disk drive error correction system comprising: a memory buffer, wherein the sector of data is stored on a magnetic hard disk (col. 8, lines 39-53).

As to claims 18-19, the claims have substantially the limitations of claim 15; therefore, they are analyzed as previously discussed in claim 15 above.

As to claims 20 and 21, the claims have substantially the limitations of claim 1 therefore, they are analyzed as previously discussed in claim 15 above.

Allowable Subject Matter

3. Claims 12 and 20-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 12 is allowable because none of the cited references either singular or in combination discloses "calculating the old cyclic redundancy check bytes based on the old LBA; storing the old cyclic redundancy check bytes in the memory buffer; and accessing the old cyclic redundancy check bytes from the memory buffer before performing the second exclusive OR function."

Claims 20 and 21 are allowable because none of the cited references either singular or in combination discloses "performing the second XOR function on a result of the Galois field multiplication and the old cyclic redundancy check bytes further comprises performing an exclusive OR function on data bytes in the sector and zero bytes."

Response to Arguments

4. Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

The Applicant asserts that Frederickson is not directed to efficiently generating "updated cyclic redundancy check bytes that are based on the new LBA, as recited in claim 1, but simply to check whether data has changed during transferring. Accordingly, there is no teaching or suggestion as to using the old CRC bytes or old LBA data to generate new updated CRC bytes based on the new LBA."

However, The Prior art of Hashemi has been used for new ground or rejection.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO-892.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

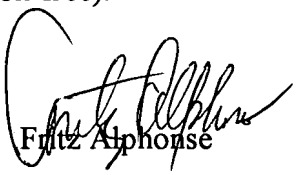
or faxed to: (703) 872-9306 for all formal communications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fritz Alphonse, whose telephone number is (571) 272-3813. The examiner can normally be reached on M-F, 8:30-6:00, Alt. Mondays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques, can be reached at (571) 272-6962.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-3824

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Fritz Alphonse

Art Unit 2112

October 10, 2007